UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,380	03/12/2004	Meikei Ieong	YOR920030394US2 (16963Z)	7287

23389 7590 06/14/2005

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,380	IEONG ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/12/2004 is acceptable.

Claim Objections

2. Claim 18 is objected to because of the following informalities: Claim 18 recites: "structure of claim 18", which violates the doctrine that a claim can not depend on itself. As best as can be understood, claim 18 depends on claim 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being obvious over Rim U.S. Patent Application Publication 20050082531.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of

invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Specifically with reference to **claim 1**, the reference discloses a hybrid substrate comprising:

a first semiconductor layer (14 or 34, Fig. 1) having a first crystallographic orientation; and

a second semiconductor layer (34 or 14) having a second crystallographic orientation which is different from the first crystallographic orientation (paragraph [0041]), wherein said first and second semiconductor layers are separated from each other by an interface (32), said second semiconductor layer has a thickness from about 2 nm to about 300 nm and said interface has an oxide thickness of about 2-500 nm.

However, the thicknesses of the various layers are different. Specifically, for said semiconductor layer, the reference discloses a thickness from about 2 nm to about 300 nm rather than about 200 nm to about 2 μm as claimed, and for the oxide, the reference discloses a thickness of about 2-500 nm rather than about 10 nm or greater as claimed.

Nevertheless, the criticality of the difference in the various thickness has not been established, therefore the change from one to another would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claim 8**, and using the same reference characters, interpretation, and citation as detailed above for claim 1 where applicable, the reference discloses an integrated semiconductor structure comprising:

a hybrid structure comprising a first device region (16) having a first crystallographic orientation (defined by layer 34) and a second device region (18) having a second crystallographic orientation (defined by layer 14), said first crystallographic orientation is different from said second crystallographic orientation, wherein at least said first device region or said second device region includes a semiconductor layer having a thickness from about 2 nm to about 300 nm and an underlying interface (12) that has an oxide thickness of about 5 nm to 500 nm or greater;

an isolation region (30) separating said first device region from said second device region; and

at least one first semiconductor device (21) located in said first device region and at least one second semiconductor device (20) located in said second device region

Referring to **claims 2 and 3**, the reference further discloses in paragraphs [0037]-[0039] that the first and the second semiconductor layers comprise materials, such as Si, SiC, and SiGe, as claimed.

Referring to **claims 4-5, 9, and 11**, the reference further discloses that said first semiconductor layer has a (100) or (110) crystal orientation and the first crystallographic

orientation is (110) or (100) and said second semiconductor layer has a (110) or (100) crystal orientation and the second crystallographic orientation is (100) or (110) (paragraph [0041]).

Referring to **claims 10 and 12**, the reference further discloses that said at least one first semiconductor device is a pFET or an nFET and said at least one second semiconductor device is an nFET or a pFET (paragraph [0041]).

Referring to **claims 6-7 and 13-17**, although the reference does not explicitly disclose that the first device region includes a regrown semiconductor material located atop a first semiconductor material, said regrown semiconductor material having the same crystallographic orientation as the first semiconductor material, the reference discloses that said first and second semiconductor layers maybe a homogeneous material or a heterogeneous structure of at least two elements stacked on top of each other – hence, regrown – and that said first and second semiconductor layers maybe strained, relaxed ("unstrained"), or a combination of strained and relaxed (paragraphs [0037]-[0040]).

With respect to **claim 18**, as mentioned above for claim 1, the reference disclose a hybrid substrate as claimed; and note that a substrate of an integrated semiconductor structure, as is known in the art, is a broadly defined sub-structure comprising everything from the bottommost element of the structure to and including source/drain regions and channel regions.

4. Claims 1-5, 8-12, and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Yeo et al. U.S. Patent Application Publication 20040195646 (the '646 reference).

The '646 reference discloses an integrated semiconductor structure, whose details are not explicitly shown, comprising a hybrid substrate (100, Fig. 1) comprising:

a first semiconductor layer (110 or 112; or 116) having a first crystallographic orientation ((100) or (110), with (100) orientation is for nFET ("n-channel transistor (not shown)") and with (110) orientation is for pFET ("p-channel transistor (not shown)", paragraph [0030]; or (110) or (100), paragraph [0037]) for the case when the first semiconductor layer is 116); and in reference to **claims 1, 4-5, and 8-12**); and

a second semiconductor layer (116, "silicon substrate"; or 110 or 112) having a second crystallographic orientation ((110) or (100)) which is different from the first crystallographic orientation ((100) or (110)), wherein said first and second semiconductor layers are separated from each other by an interface (114, "silicon oxide", paragraph [0036]), said second semiconductor layer (116) has an unspecified thickness or (110 or 1112) has a thickness of about 1-100 nm (paragraph [0033]) and said interface has an oxide thickness of about 10 nm to 200 nm (100 angstroms to 2000 angstroms, paragraph [0036]).

However, the thicknesses of the various layers are different. Specifically, for said semiconductor layer, the reference discloses a thickness from about 1 nm to about 100 nm rather than about 200 nm to about 2 μm as claimed, and for the oxide, the reference discloses a thickness of about 10-200 nm rather than about 10 nm or greater as claimed.

Nevertheless, the criticality of the difference in the various thickness has not been established, therefore the change from one to another would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claim 8**, and using the same reference characters, interpretation, and citation as detailed above for claim 1 where applicable, the reference discloses an integrated semiconductor structure comprising:

a hybrid structure comprising a first device region (generally defined by the section of the substrate 100 generally defined by the layer 110) having a first crystallographic orientation (defined by layer 110 or that portion of layer 116) and a second device region (generally defined by the section of the substrate 100 generally defined by the layer 112) having a second crystallographic orientation (defined by layer 112 or that portion of layer 116), said first crystallographic orientation is different from said second crystallographic orientation, wherein at least said first device region or said second device region includes a semiconductor layer (110 or 112) having a thickness from about 1-100 nm (110 or 112) and an underlying interface (114) that has an oxide thickness of about 10-200 nm;

an isolation region (not shown in Fig. 1, but should be present for the device to function, similarly to isolation 178 shown in Figs. 9) separating said first device region from said second device region; and

at least one first semiconductor device (nFET or pFET, not shown, as noted above) located in said first device region and at least one second semiconductor device (pFET or nFET, not shown, as noted above) located in said second device region

Referring to **claims 2 and 3**, the reference further discloses in paragraphs [0029] and [0037] that the first and the second semiconductor layers comprise silicon, satisfying the materials of the claimed Markush group of materials..

Referring to **claims 4-5, 9, and 11**, as noted above, the reference further discloses that said first semiconductor layer has a (100) or (110) crystal orientation and the first crystallographic orientation is (110) or (100) and said second semiconductor layer has a (110) or (100) crystal orientation and the second crystallographic orientation is (100) or (110).

Referring to **claims 10 and 12**, as noted above, the reference further discloses that said (not-shown) at least one first semiconductor device is a pFET or an nFET and said (not-shown) at least one second semiconductor device is an nFET or a pFET.

With respect to **claim 18**, as mentioned above for claim 1, the reference disclose a hybrid substrate as claimed; and note that a substrate of an integrated semiconductor structure, as is known in the art and as disclosed explicitly by the reference, is a broadly defined sub-structure comprising everything from the bottommost element of the structure to and including source/drain regions and channel regions.

5. **Claims 1-7 are** rejected under 35 U.S.C. 103(a) as being obvious over Maeda et al. U.S. Patent Application Publication 20040075141 (the '141 reference).

Referring to **claim 1**, the reference discloses a hybrid substrate comprising:

a first semiconductor layer (1 or 3b, Fig. 22) having a first crystallographic orientation (<110> or <100>); and

a second semiconductor layer (3b or 1) having a second crystallographic orientation (<100> or <110>) which is different from the first crystallographic orientation, wherein said first and second semiconductor layers are separated from each other by an interface (2), said second semiconductor layer has an unspecified thickness and said interface has an oxide of an unspecified thickness.

However, the thicknesses of the various layers are different. Specifically, for said semiconductor layer, the reference does not disclose a thickness instead of the claimed about 200

nm to about 2 μm, and for the oxide, the reference also does not discloses a thickness instead of the claimed about 10 nm or greater.

Nevertheless, the criticality of the difference in the various thickness has not been established, especially the change from an unspecified one to a specific but uncritical one would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to **claims 2 and 3**, the reference further discloses in paragraph [0118] that the first and the second semiconductor layers comprise materials, such as Si and SiGe, meeting the claimed Markush group of materials.

Referring to **claims 4-5**, as noted above, the reference further discloses that said first semiconductor layer has a (100) or (110) crystal orientation and said second semiconductor layer has a (110) or (100) crystal orientation.

Referring to **claims 6-7**, the reference further discloses in paragraph [0118] that said first (3b) and second (3b) semiconductor layers each comprises a relaxed semiconductor material (unspecified or unstrained layer 31 relaxed by strained layer 32) or a stack of a relaxed semiconductor material (31) and a strained semiconductor material (32).

6. **Claims 8-18 are** rejected under 35 U.S.C. 103(a) as being obvious over Maeda et al. U.S. Patent Application Publication 20040075141 (the '141 reference) or further in view of Yeo et al. U.S. Patent Application Publication 20040195646 (the '646 reference).

The '141 reference discloses in the "fifth aspect", paragraph [0024], that channel direction of N-channel transistors are aligned parallel to a <100> crystal direction of the SOI layer and that channel direction of P-channel transistors are aligned parallel to a <110> crystal

direction of the SOI layer; the fifth aspect, therefore, in junction with the first aspect that teaches that the support substrate (the layer, for example layer 1 as detailed above for claims 1-7, that is separated from the SOI layer, for example layer 3b also as detailed above, by the so-called buried oxide, for example layer 2 also as detailed above) and the SOI layer have different crystal orientations with respect to each other (paragraph [0016]) teaches all limitations as recited in **claim 8**. And this fifth/first aspects, modified in view of the sixth preferred embodiment, detailed above, creating a relaxed semiconductor material (unspecified or unstrained layer 31 relaxed by strained layer 32) or a stack of a relaxed semiconductor material (31) and a strained semiconductor material (32), detailed above, for the purpose of improving carrier mobility (paragraph [0121]), meeting the limitations of **claims 9-18**.

Or; the '141 reference discloses in the first aspect, as detailed above, that the support substrate (the layer, for example layer 1 as detailed above for claims 1-7, that is separated from the SOI layer, for example layer 3b also as detailed above, by the so-called buried oxide, for example layer 2 also as detailed above) and the SOI layer have different crystal orientations with respect to each other (paragraph [0016]). This first aspect, applied in forming the structure of Fig. 19 of the fifth embodiment to have at least a p-channel transistor and at least an n-channel transistor and modified in view of the teachings of the '646 reference that crystallographic orientation of (100) is suitable for forming an n-channel transistor and crystallographic orientation of (110) is suitable for forming an p-channel transistor (the '646 reference, paragraph [0030]) teaches all limitations as recited in **claim 8**. And this first aspect/fifth embodiment/modified-in-view-of-the-'646-reference, modified in view of the sixth preferred embodiment, detailed above, creating a relaxed semiconductor material (unspecified or

unstrained layer 31 relaxed by strained layer 32) or a stack of a relaxed semiconductor material (31) and a strained semiconductor material (32), detailed above, for the purpose of improving carrier mobility (paragraph [0121]), meeting the limitations of **claims 9-18**.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
May 24, 2005